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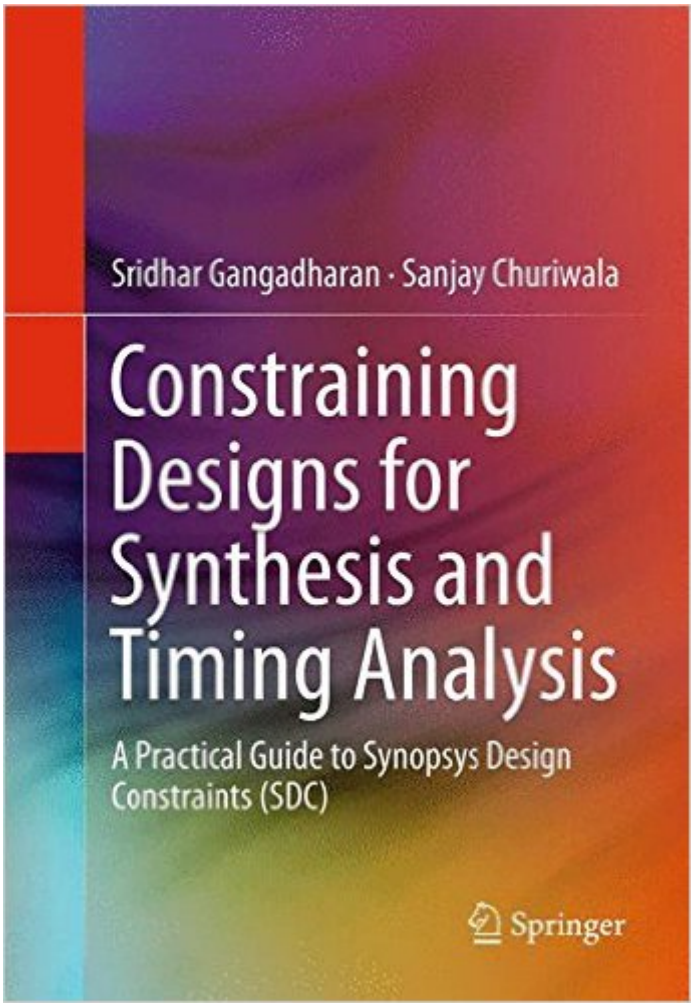
# Constraining Designs For Synthesis And Timing Analysis: A Practical Guide To Synopsys Design Constraints (SDC)

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## Synopsis

This book serves as a hands-on guide to timing constraints in integrated circuit design.Â  Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly.Â  Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing.Â  Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

## Book Information

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## Customer Reviews

An excellent handbook for Synopsys Design Constraints (SDC). The context in which the SDCs are typically used is nicely explained. It becomes very useful for people like me (EDA engineers) who have to understand how the designers use the Constraints in their world. Most material on SDCs are about the different options that a particular SDC has, but never explains clearly why one might use the option.

I was very disappointed with this book, considering the price. I was hoping for some more detailed real world examples. The level of detail presented can just be found with some simple google searching.

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